Project Title

INTELLERA,

A Hardware based Acceleration of Matrix MAC Processor.

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***Please note that there are many figures that you have to draw. I have only included two.***

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# INTRODUCTION

## PURPOSE

In the field of machine learning, matrix multiplication is a fundamental operation that plays a crucial role in various algorithms and computations. However, traditional processors often struggle to efficiently execute matrix multiplication tasks due to their general-purpose nature. This inefficiency results in increased time consumption and hampers the overall performance of machine learning applications. Therefore, there is a pressing need for a specialized processor design that incorporates matrix multiplication as a core instruction and aims to decrease time consumption in machine learning.

## PRODUCT SCOPE

Intellera is a groundbreaking project aimed at designing a RISC-V based processor with a customized instruction set architecture (ISA) that includes matrix multiplication instructions. The goal of Intellera is to address the performance bottleneck caused by conventional processors when executing matrix operations in machine learning algorithms. By enhancing the processor's capabilities and providing dedicated hardware acceleration for matrix Multiply-Accumulate (MAC) operations, Intellera aims to significantly reduce the time consumed in machine learning tasks.

Intellera proposes a novel approach to address the time consumption challenge in machine learning. The project focuses on designing a RISC-V based processor that features an extended instruction set architecture specifically tailored for matrix multiplication. By integrating dedicated hardware support for matrix MAC operations, Intellera can harness the parallel(pipelining) processing capabilities of the processor to accelerate matrix computations and reduce the overall execution time.

The project utilizes the knowledge of computer hardware and Risc-V Instruction Set for creating a customized instruction set and concept of systolic arrays implementation for accelerating the multiplication of matrices.

Table 1: Terms used in this document and their description.

|  |  |
| --- | --- |
| Name | Description |
| RISC | Reduced Instruction Set Computer |
| FPGA | Field Programable Gate Array |
| ISA | Instruction Set Architecture |
| MAC | Multiplication Accumulation |
| ALU | Arithmetic Logic Unit |

## OVERVIEW

The "FPGA-Based RISC-V Processor with Matrix MAC Module" project represents a cutting-edge venture in the realm of digital systems design and high-performance computing. This project combines the versatility of the RISC-V instruction set architecture (ISA) with the computational power of specialized Matrix Multiply-Accumulate (MAC) operations. The overarching goal is to create a flexible and high-performance computing platform that can efficiently handle a wide range of computational tasks, including those heavily reliant on matrix operations, such as machine learning, signal processing, and scientific computing.

## Key Objectives

1. RISC-V Processor Integration: The project's foundation rests on the integration of a 32-bit RISC-V processor, adhering to the RV32I standard. This serves as the backbone for executing standard RISC-V instructions.
2. Custom ISA for Matrix Operations: A custom instruction set architecture (ISA) optimized for matrix operations is developed and integrated into the processor. This custom ISA includes Matrix MAC instructions, enabling precise and efficient matrix multiplication and addition.
3. High-Performance Computing: The processor is designed with a keen focus on performance. It aims to achieve high clock frequencies and low-latency execution to support real-time and computationally intensive tasks.
4. Hardware Pipelining: To improve instruction throughput, the processor employs a pipelining architecture with at least five stages, optimizing the execution of instructions.
5. FPGA Implementation: The project leverages Field-Programmable Gate Arrays (FPGAs) as the hardware platform for development and testing. FPGA compatibility allows for rapid prototyping and real-time testing of the processor's capabilities.
6. Software Toolchain Integration: The project integrates with software tools like Vivado for hardware description and synthesis, Venus for assembly code development, and DigitalJS for schematic design.

## Expected Outcomes

The successful realization of this project will yield a versatile FPGA-based computing platform capable of executing both standard RISC-V instructions and custom Matrix MAC operations. This system's adaptability, high-performance characteristics, and FPGA compatibility position it as an ideal choice for various applications across domains, ranging from embedded systems to scientific research.

# THE OVERALL DESCRIPTION

The project encompasses the development of a versatile RISC-V processor with the primary objective of accelerating matrix multiplication operations, a pivotal task within the domain of machine learning and scientific computing. The project's evolution began with the implementation of a single-cycle RISC-V processor using Vivado, establishing a solid foundation for subsequent enhancements. The immediate plan involves transitioning this processor into a highly efficient, pipelined architecture with five stages. This pipeline design aims to mitigate hazards and optimize the execution of RISC-V instructions, delivering improved throughput and performance. Beyond the processor core, a key innovation lies in the integration of a dedicated systolic array hardware architecture, meticulously designed to expedite matrix multiplication. This addition introduces a specialized matrix computation engine, effectively harnessing parallelism to dramatically reduce execution times for large-scale matrix operations.

## 2.1. PRODUCT PERSPECTIVE

In the realm of modern computing, the demand for high-performance processors tailored to specific computational tasks has intensified. The customized RISC-V processor represents an innovative response to this demand, offering a scalable and efficient solution for accelerating matrix multiplication operations. It stands at the intersection of hardware and software, where traditional RISC-V architecture is enhanced with a carefully crafted module inspired by systolic array for matrix operations. This project is a testament to the adaptability and extensibility of the RISC-V ISA, providing a dedicated solution for a critical computation within machine learning workflows. It complements existing processors by offering superior matrix computation capabilities, making it an invaluable tool for a wide range of applications, including deep learning, data analytics, and scientific simulations.

# WORK BREAKDOWN STRUCTURE

Figure 1 Work Breakdown Structure

# Design

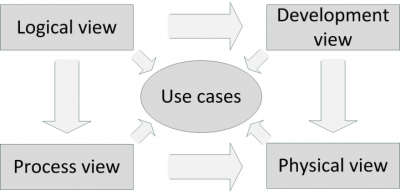
## ARCHITECTURAL DESIGN

## Why we choose ????? Architecture Design?

## MODULE IDENTIFICATION

# 4+1 ARCHITECTURE VIEW MODEL

In this section, you draw the architecture using the views defined in the “4+1” model.



5 4+1 Architecture View

## Use Case View

This is a list of use-cases that represent major functionality of the final system:

## Logical View:

## Development View

## Process View

## Physical View

## User Interface Design